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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/004,338	11/14/2001	Seungyoon Peter Song	2214P	4959

7590 09/28/2004

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EXAMINER	
COLEMAN, ERIC	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 09/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/004,338	SONG, SEUNGYOON PETER	
	Examiner	Art Unit	
	Eric Coleman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,15-21 and 24-29* is/are rejected.

7)☒ Claim(s) *10-14,22 and 23* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-3,9,15-21,24,25,28,29 are rejected under 35 U.S.C. 103(a) as being unpatentable over (Witt patent No. 6,240,503) (hereafter referred to as Witt '503) in view of Brown (patent No. 5,488,730).

3. Witt '503 taught the invention substantially as claimed including a data processing ("DP") system comprising:

a) Pairs of future state (76) and architectural state pointers (78)(e.g., see fig.3, col. 17, lines 45-62 and col. 18, line 39-col. 19, line 6);

b) Operand queue (84) including at least one entry (e.g., see fig. 3 and col. 18, lines 46-64).

4. Witt '503 did not expressly detail (claims 1, 25) a reference counter associated with each operand queue entry. Brown however taught reference counters associated with each operand entry in queues (e.g., see col. 24, line 59-col. 25, line 10 and col. 26, line 39-col. 27, line 42) Brown also taught operand queue (79)(e.g., see col. 13, lines 54-64).

5. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Witt '503 and Brown. One of ordinary skill would have bee motivated to

incorporate the Brown teachings of counters for the operand queues in order to reduce the amount of circuitry needed to keep track of a large number of register dependencies and in particular keep track of multiple dependencies to a single register (e.g., see col. 3, lines 16-52).

6. As per claim 2,28 Brown taught a free operand entry is assigned to hold a future value of a register by writing the free entry's number into the register's future state pointer and incrementing the free entry's reference count (e.g., see col. 26, line 54-col. 27,line 42).

7. As per claim 3,29 Brown taught the assigned entry number is written to the register's architectural state pointer and the reference count of the entry previously assigned to the register is decremented upon completed of the instruction (e.g., see col. 27, line 1-42).

As per claims 9,18 Brown taught a cancelled instruction does not modify associated architectural state pointer but the reference count of the entry assigned to the register is decremented (e.g., see col. 27, lines 22-42).

8. As per claim 15,16,17,19 Witt and Brown did not expressly detail how to process dependencies when at least one operand was immediate. However one of ordinary skill would have been motivated to allocate a entry in the operand queue for an immediate operand (with incrementing/decrementing the counter) at least because a conflict in the destination registers may happen as Brown maintains source and destination queues (e.g., see col. 12, line 58-col. 13, line 15). Also the only time requirement to write the immediate operand would have been to write the operand before the operand was

needed to be read (this would have encompassed immediate writing and decrementing and/or delays in writing and/or decrementing that would not conflict with the read).

9. As per claim 20, Witt and Brown did not specify how the architectural and future state pointer were handled in a multithreaded implementation. However, since in a multithreaded implementation there would have been the need to separate the registers used in each respective thread from the registers used in another thread for coherency of the data then one of ordinary skill would have been motivated to maintain separate separate future state and architectural state registers and pointers for each thread and the processor processing the thread.

10. As per claim 21, Brown taught the storing of value in the future state pointers and architectural state pointers (source and destination queues) without regard to the value of the operand (e.g., see col. 26, line 54-col. 27,line 42).

11. As to the limitations of claim 24, Brown taught that the counters decremented on a when a entry was remove from the queue and detected a counter value of zero for preventing a read of the values in the queue. This procedure would have required decrementing the counter when the last entry was removed from the queue so that the counter would contain a zero value (e.g., see col. 27, lines 23-43 of Brown).

12. Claims 4-8,26,27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Witt '503 in view of Brown as applied to claims 1-3 above, and further in view of Thomas (patent No. 5,535,346).

13. Thomas taught (as to claim 4,5,26,27) each register is assigned a unique operand queue entry upon a reset (e.g., see col. 7, lines 27-48) and all registers that have an undefined value (such as a result of divide by zero) upon reset are assigned to at least one operand queue entry and each of the registers that have defined value upon reset is assigned a unique entry upon a reset (e.g., see col. 7, lines 27-48).

14. It would have been obvious to one of ordinary skill to combine the teachings of Thomas and Witt '503. One of ordinary skill would have been motivated to incorporate the Thomas teachings of a future file control that corrects the future file in a single cycle as least to provide for a more efficient recovery from processing errors or system errors (e.g., see col. 7, lines 27-48 of Thomas).

15. As per claim 6, Thomas taught the entry number previously assigned to the register is obtained from the register's future state pointer (e.g., see col. 2, lines 41-50).

16. As to claim 7, Thomas the entry number previously assigned to the register is obtained from the register's architectural state pointer (e.g., see col. 9, lines 12-67).

17. As to claim 8, Thomas taught in which each the architectural state pointer is copied to its corresponding future pointer when processing an exception condition (e.g., see col. 9, lines 12-67).

Allowable Subject Matter

18. Claims 10-14,22,23 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Williamson (patent No. 6,192,461) disclosed a system for facilitating multiple storage instruction completions in a superscalar processor during a single clock cycle (e.g., see abstract).

Witt (patent No. 6,237,082) disclosed a recorder buffer configured to allocate storage for instruction results corresponding to predefined maximum number of concurrently receivable instructions independent of a number of instructions received (e.g., see abstract).

Farrell (patent No. 6,167,508) disclosed a register scoreboard logic with register read availability signal to reduce instruction issue arbitration latency (e.g., see abstract).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (703) 305-9674 or (571) 272-4163. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EC

ERIC COLEMAN
PRIMARY EXAMINER